# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 9 | (((full or falf) near3 cycle) near10 encod$3) with (transmit$4 or send or receiv$3 or receipt$3) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/25 15:53 |
| L2 | 13495 | ((cycle or cyclic or period or interval or portion or wave or waveform or wave-form) near10 encod$3) with (transmit$4 or send or receiv$3 or receipt$3) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/25 15:54 |
| L3 | 145664 | data with ((time or timing) near3 (period or interval)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/25 15:54 |
| L4 | 732 | 2 same 3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/25 15:55 |
| L5 | 2583 | 2 and 3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/25 15:55 |
| L6 | 14989 | (375/219 or 375/222 or 375/242 or 375/244 or 375/254 or 375/257 or 375/259 or 375/265 or 375/295 or 375/354 or 375/362 or 375/364).ccls. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/25 15:56 |
| L7 | 53 | 4 and 6 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/25 15:56 |
| L8 | 194 | 5 and 6 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/25 15:56 |

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## Inventor Name Search Result

Your Search was:

Last Name = GRIFFIN
First Name = JED

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 09475261 | 6411132 | 150 | 12/30/1999 | MATCHED CURRENT DIFFERENTIAL AMPLIFIER | GRIFFIN, JED |
| 09476425 | 6400176 | 150 | 12/30/1999 | CONSTANT CMOS DRIVER | GRIFFIN, JED |
| 09608529 | 6624659 | 150 | 06/30/2000 | DYNAMICALLY UPDATING IMPEDANCE COMPENSATION CODE FOR INPUT AND OUTPUT DRIVERS | GRIFFIN, JED |
| 09939763 | 6489821 | 150 | 08/28/2001 | HIGH FREQUENCY SYSTEM WITH DUTY CYCLE BUFFER | GRIFFIN, JED |
| 10113485 | 6515503 | 150 | 04/01/2002 | CMOS APPARATUS FOR DRIVING TRANSMISSION LINES | GRIFFIN, JED |
| 10277968 | 6621313 | 150 | 10/23/2002 | HIGH FREQUENCY SYSTEM WITH DUTY CYCLE BUFFER | GRIFFIN, JED |
| 11075491 | Not Issued | 41 | 03/08/2005 | Temperature sensing | GRIFFIN, JED |
| 09749661 | 6791412 | 150 | 12/28/2000 | DIFFERENTIAL AMPLIFIER OUTPUT STAGE | GRIFFIN, JED D. |
| 09750132 | 6498539 | 150 | 12/29/2000 | HIGHLY ACCURATE VOLTAGE CONTROLLED OSCILLATORS WITH RC CIRCUIT | GRIFFIN, JED D. |
| 10225691 | 7158594 | 150 | 08/21/2002 | RECEIVERS FOR CONTROLLED FREQUENCY SIGNALS | GRIFFIN, JED D. |
| 10226074 | Not Issued | 71 | 08/21/2002 | Controlled frequency signals | GRIFFIN, JED D. |
| 10625944 | Not Issued | 30 | 07/23/2003 | Receivers for cycle encoded signals | GRIFFIN, JED D. |
| 10625945 | Not Issued | 30 | 07/23/2003 | Transmitters providing cycle encoded signals | GRIFFIN, JED D. |

| | | | | | |
|---|---|---|---|---|---|
| 11088445 | Not Issued | 25 | 03/23/2005 | On-die temperature monitoring in semiconductor devices to limit activity overload | GRIFFIN, JED D. |
| 11241550 | Not Issued | 30 | 09/30/2005 | Dual-reference delay-locked loop (DLL) | GRIFFIN, JED D. |
| 11476948 | Not Issued | 30 | 06/28/2006 | System to calibrate on-die temperature sensor | GRIFFIN, JED D. |
| 09108606 | 6137317 | 150 | 07/01/1998 | CMOS DRIVER | GRIFFIN, JED D. |

Inventor Search Completed: No Records to Display.

**Search Another: Inventor** **Last Name** GRIFFIN **First Name** JED Search

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## Inventor Name Search Result

Your Search was:

Last Name = JEX
First Name = JERRY

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 08315284 | 5539739 | 150 | 09/29/1994 | ASYNCHRONOUS INTERFACE BETWEEN PARALLEL PROCESSOR NODES | JEX, JERRY |
| 08375361 | 5598113 | 150 | 01/19/1995 | FULLY ASYNCHRONOUS INTERFACE WITH PROGRAMMABLE METASTABILITY SETTLING TIME SYNCHRONIZER | JEX, JERRY |
| 09676313 | 6384658 | 150 | 09/29/2000 | Clock splitter circuit to generate synchronized clock and inverted clock | JEX, JERRY G. |
| 09820899 | 6466074 | 150 | 03/30/2001 | LOW SKEW MINIMIZED CLOCK SPLITTER | JEX, JERRY G. |
| 10002418 | 6549031 | 150 | 11/13/2001 | POINT TO POINT ALTERNATING CURRENT (AC) IMPEDANCE COMPENSATION FOR IMPEDANCE MISMATCH | JEX, JERRY G. |
| 10128615 | 7050507 | 150 | 04/22/2002 | ADAPTIVE THROUGHPUT PULSE WIDTH MODULATION COMMUNICATION SCHEME | JEX, JERRY G. |
| 10225691 | 7158594 | 150 | 08/21/2002 | RECEIVERS FOR CONTROLLED FREQUENCY SIGNALS | JEX, JERRY G. |
| 10226074 | Not Issued | 71 | 08/21/2002 | Controlled frequency signals | JEX, JERRY G. |
| 10625944 | Not Issued | 30 | 07/23/2003 | Receivers for cycle encoded signals | JEX, JERRY G. |
| 10625945 | Not Issued | 30 | 07/23/2003 | Transmitters providing cycle encoded signals | JEX, JERRY G. |
| 07861093 | 5267213 | 150 | 03/31/1992 | BIAS CIRCUITRY FOR CONTENT ADDRESSABLE MEMORY CELLS OF A | JEX, JERRY G. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | FLOATING GATE NONVOLATILE MEMORY | |
| 07861473 | Not Issued | 166 | 04/01/1992 | APPARATUS AND METHOD FOR FAST PROGRAM, ERASE, AND REPAIR SEQUENCES FOR A NONVOLATILE SEMICONDUCTOR MEMORY | JEX, JERRY G. |
| 07971074 | 5309012 | 150 | 11/03/1992 | PROTECTED ERASE VOLTAGE DISCHARGE TRANSISTOR IN A NONVOLATILE SEMICONDUCTOR MEMORY | JEX, JERRY G. |
| 08296019 | 5623644 | 150 | 08/25/1994 | POINT-TO-POINT PHASE-TOLERANT COMMUNICATION | JEX, JERRY G. |
| 08307502 | 5434892 | 150 | 09/16/1994 | THROTTLING CIRCUIT FOR A DATA TRANSFER SYSTEM | JEX, JERRY G. |
| 08361872 | 5506803 | 150 | 12/22/1994 | APPARATUS AND METHOD FOR MINIMIZING VERIFY TIME IN A SEMICONDUCTOR MEMORY BY CONSTANTLY CHARGING N-WELL CAPACITANCE | JEX, JERRY G. |

Inventor Search Completed: No Records to Display.

**Search Another: Inventor** **Last Name** JEX **First Name** JERRY Search

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## Inventor Name Search Result

Your Search was:

Last Name = FORESTIER
First Name = ARNAUD

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 10002418 | 6549031 | 150 | 11/13/2001 | POINT TO POINT ALTERNATING CURRENT (AC) IMPEDANCE COMPENSATION FOR IMPEDANCE MISMATCH | FORESTIER, ARNAUD |
| 10608633 | 6922077 | 150 | 06/27/2003 | HYBRID COMPENSATED BUFFER DESIGN | FORESTIER, ARNAUD |
| 10869573 | 7043392 | 150 | 06/16/2004 | INTERPOLATOR TESTING SYSTEM | FORESTIER, ARNAUD |
| 10879676 | 7009431 | 150 | 06/29/2004 | INTERPOLATOR LINEARITY TESTING SYSTEM | FORESTIER, ARNAUD |
| 11000699 | 7071728 | 150 | 11/30/2004 | HYBRID COMPENSATED BUFFER DESIGN | FORESTIER, ARNAUD |
| 10128615 | 7050507 | 150 | 04/22/2002 | ADAPTIVE THROUGHPUT PULSE WIDTH MODULATION COMMUNICATION SCHEME | FORESTIER, ARNAUD J. |
| 10625944 | Not Issued | 30 | 07/23/2003 | Receivers for cycle encoded signals | FORESTIER, ARNAUD J. |
| 10625945 | Not Issued | 30 | 07/23/2003 | Transmitters providing cycle encoded signals | FORESTIER, ARNAUD J. |

Inventor Search Completed: No Records to Display.

**Search Another: Inventor** Last Name: FORESTIER First Name: ARNAUD Search

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## Inventor Name Search Result

Your Search was:

Last Name = VAKIL
First Name = KERSI

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 10002418 | 6549031 | 150 | 11/13/2001 | POINT TO POINT ALTERNATING CURRENT (AC) IMPEDANCE COMPENSATION FOR IMPEDANCE MISMATCH | VAKIL, KERSI |
| 10798557 | Not Issued | 30 | 03/12/2004 | System and method for automatically calibrating two-tap and multi-tap equalization for a communications link | VAKIL, KERSI |
| 09820899 | 6466074 | 150 | 03/30/2001 | LOW SKEW MINIMIZED CLOCK SPLITTER | VAKIL, KERSI H. |
| 10128615 | 7050507 | 150 | 04/22/2002 | ADAPTIVE THROUGHPUT PULSE WIDTH MODULATION COMMUNICATION SCHEME | VAKIL, KERSI H. |
| 10625944 | Not Issued | 30 | 07/23/2003 | Receivers for cycle encoded signals | VAKIL, KERSI H. |
| 10625945 | Not Issued | 30 | 07/23/2003 | Transmitters providing cycle encoded signals | VAKIL, KERSI H. |
| 10869573 | 7043392 | 150 | 06/16/2004 | INTERPOLATOR TESTING SYSTEM | VAKIL, KERSI H. |
| 10879676 | 7009431 | 150 | 06/29/2004 | INTERPOLATOR LINEARITY TESTING SYSTEM | VAKIL, KERSI H. |
| 10879788 | 7019550 | 150 | 06/29/2004 | LEAKAGE TESTING FOR DIFFERENTIAL SIGNAL TRANSCEIVER | VAKIL, KERSI H. |
| 10881097 | Not Issued | 30 | 06/29/2004 | Various methods and apparatuses for lane to lane deskewing | VAKIL, KERSI H. |
| 10935903 | Not Issued | 30 | 09/07/2004 | Training pattern for a biased clock recovery tracking loop | VAKIL, KERSI H. |
| 11375498 | Not Issued | 30 | 03/13/2006 | Input/output agent having multiple secondary ports | VAKIL, KERSI H. |
| 11541427 | Not | 19 | 09/29/2006 | Dual clock domain deskew circuit | VAKIL, KERSI H. |

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# Inventor Search Completed: No Records to Display.

**Search Another: Inventor**

| Last Name | First Name | |
|---|---|---|
| VAKIL | KERSI | Search |

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## Inventor Name Search Result

Your Search was:

Last Name = KOLLA
First Name = ABHIMANYU

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 10002418 | 6549031 | 150 | 11/13/2001 | POINT TO POINT ALTERNATING CURRENT (AC) IMPEDANCE COMPENSATION FOR IMPEDANCE MISMATCH | KOLLA, ABHIMANYU |
| 10128615 | 7050507 | 150 | 04/22/2002 | ADAPTIVE THROUGHPUT PULSE WIDTH MODULATION COMMUNICATION SCHEME | KOLLA, ABHIMANYU |
| 10625944 | Not Issued | 30 | 07/23/2003 | Receivers for cycle encoded signals | KOLLA, ABHIMANYU |
| 10625945 | Not Issued | 30 | 07/23/2003 | Transmitters providing cycle encoded signals | KOLLA, ABHIMANYU |
| 10733100 | Not Issued | 30 | 12/10/2003 | Non-integer word size translation through rotation of different buffer alignment channels | KOLLA, ABHIMANYU |
| 10869573 | 7043392 | 150 | 06/16/2004 | INTERPOLATOR TESTING SYSTEM | KOLLA, ABHIMANYU |
| 10879676 | 7009431 | 150 | 06/29/2004 | INTERPOLATOR LINEARITY TESTING SYSTEM | KOLLA, ABHIMANYU |
| 10935902 | Not Issued | 30 | 09/07/2004 | Training pattern based de-skew mechanism and frame alignment | KOLLA, ABHIMANYU |
| 11375498 | Not Issued | 30 | 03/13/2006 | Input/output agent having multiple secondary ports | KOLLA, ABHIMANYU |
| 11541427 | Not Issued | 19 | 09/29/2006 | Dual clock domain deskew circuit | KOLLA, ABHIMANYU |
| 60111657 | Not Issued | 159 | 12/10/1998 | ADDRESSABLE ARRAY OF MICROELECTRODES WITH EMBEDDED ELECTRONICS FOR NEURAL RECORDING | KOLLA, ABHIMANYU |

Inventor Search Completed: No Records to Display.

**Last Name** **First Name**

**Search Another: Inventor** KOLLA ABHIMANYU Search

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